REMARKS

The objections to the drawings have been complied with. Numerals 150 and 152 have been added to the specification. A replacement sheet for Figure 9 is enclosed herewith.

The title has been amended.

The rejection of claims 13 and 15 - 19 under 35 USC 103 over Agahi in view of Hummler is respectfully traversed, since the combination of references does not meet the limitations of the claims.

Claims 13 and 19 have been amended. Support is found in paragraphs 29 and 36.

Applicants readily agree that Agahi shows a trench DRAM cell having an epitaxially deposited transistor body. Applicants point out, however, that Agahi does not show "a vertical body layer of strained silicon formed on an exposed vertical surface within the trench". Applicants point out that Figure 7 of Agahi shows a layer of silicon 203 having a vertical surface on which is deposited a layer of epi 222 that is described in Column 4, lines 7 - 8 as "the signal transfer region 222 is an epitaxial silicon region".

Thus, both materials are the same (silicon) and there is no strain.

In contrast, claims 13 and 19 require that the layer deposited on is SiGe and that the epi layer is silicon. As is well known, that combination produces a significant strain that has a significant effect on the transistor mobility.

An additional point is that there is no overhang of a pad dielectric in Agahi's example to produce the vertical surface being recessed from the original trench width, as required by the amended claims 13 and 19.

Applicants call the Examiner's attention to Fig. 7 of Agahi, showing that the edge of pad nitride 242 is perfectly in line with the vertical surface of layer 203; indeed, transistor body 222 overlaps the layer 203 and pad nitride 242 perfectly.

Applicants readily agree that the Hummler reference shows a trench DRAM cell and the use of SiGe in Col 4, lines 24 - 35.

Applicants point out, however, that Hummler does not teach the use of an epitaxial transistor body deposited on the vertical surface of the trench.

Since the two references show a) an epi transistor body of the same material as the surface it is deposited on; and b) a SiGe layer with an ordinary vertical transistor construction (no epi body) the combination of the two references does not teach or suggest the invention defined by the claims.

In addition, the use of an epitaxial transistor body having a thickness such that it fills the recess in the upper part of the trench (so that voids do not form under the pad overhang when filling the trench with the gate electrode) is not taught or suggested by either of the references.

The rejection of claims 14 and 20 under 35 USC 103 is also respectfully traversed. Claims 14 and 20 have been amended. Support is found in paragraph 22.

The foregoing arguments also apply to these claims, since they are dependent. In addition, the Examiner has stated "The buffer layer (in the Imai reference) is SiGe between the substrate and other SiGe layer to form tensile strain and improve speed (Column 4, lines 48 - 65)". Applicants agree with the examiner on this point.

Applicants point out, however, that the buffer layer 20 in the present invention is interposed to displace the inevitable crystal defects caused by the difference in atomic structure between the bulk silicon and the SiGe

layer from the region of the vertical transistor (paragraph 22), so that the SiGe layer 30 is fully relaxed. Therefore since the layer 30 is fully relaxed, the improvement in performance of the transistor comes from the strain that results from the difference between the fully relaxed SiGe layer and the strained silicon transistor body.

This is totally different from the operation of the reference as described by the Examiner, where the buffer layer causes strain.

For the foregoing reasons, allowance of the claims is respectfully solicited.

Respectfully submitted,

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